Claims

What is claimed is:

1. A method of treating a semiconductor device, comprising:

providing a capacitor having a first plate, a dielectric over said first plate, and a first conductive layer over said dielectric; and

exposing said first conductive layer to an N_2/H_2 plasma.

2. The method in claim 1, wherein said step of providing a capacitor comprises providing an in-process capacitor; and said method further comprises a step of providing a second conductive layer over said first conductive layer.

3. The method in claim 2, further comprising a step of defining a top plate with said first conductive layer and said second conductive layer.

4. A method of passivating a conductive material, comprising:

providing said conductive material, wherein said conductive material has an ability to associate with oxygen; and

exposing said conductive material to a plasma.

5. The method in claim 4, wherein said step of exposing said conductive material to a plasma causes a reduction in said ability of said conductive material to associate with oxygen.

6. The method in claim 4, wherein said step of exposing said conductive material to a plasma comprises exposing said conductive material to a plasma containing a selection of nitrogen and hydrogen.

7. The method in claim 6, wherein said step of exposing said conductive material to a plasma containing nitrogen comprises exposing said conductive material to a plasma selected from a group consisting of an N_2/H_2 plasma, an N_2 plasma, an H_2 plasma, an NH_3 plasma, and mixtures thereof.

8. The method in claim 7, wherein said step of exposing said conductive material to a plasma containing nitrogen comprises exposing said conductive material to an N_2/H_2 plasma under parameters including:

a temperature ranging from about 150 to about 600 degrees Celsius;

an H_2 gas flow of about 50 to about 2000 sccm;

an N_2 gas flow of about 5 to about 1000 sccm;

an Ar gas flow of about 200 to about 2000 sccm;

an RF power ranging from about 50 to about 1000W;

a pressure ranging from about 1 millitorr to about 10 torr; and

a process time ranging from about 10 seconds to about 240 seconds.

9. The method in claim 7, wherein said step of exposing said conductive material to a plasma containing nitrogen comprises exposing said conductive material to an NH_3 plasma under parameters including:

a temperature ranging from about 150 to about 600 degrees Celsius;

an NH_3 gas flow of about 5 to about 1000 sccm;

an Ar gas flow of about 200 to about 2000 sccm;

an RF power ranging from about 50 to about 1000W;

a pressure ranging from about 1 millitorr to about 10 torr; and

a process time no greater than about 500 seconds.

10. A method of affecting a surface of a conductive layer included as part of a capacitor plate, comprising:

introducing an oxygen-free material to said conductive layer of said capacitor; and

passivating said surface with said oxygen-free material.

11. The method in claim 10, wherein said step of introducing an oxygen-free material comprises introducing a gas containing said oxygen-free material.

12. The method in claim 11, wherein said step of introducing a gas comprises introducing a generally un-ionized gas.

13. The method in claim 12, wherein said step of introducing a generally un-ionized gas comprises providing a nitrogen-free gas.

14. The method in claim 12, wherein said step of introducing a generally un-ionized gas comprises providing a gas selected from a group consisting of ammonia, diborane, phosphine, hydrazine, monomethylhydrazine, carbon tetrafluoride , CHF_3, HCl, boron trichloride, carbon-silicon compounds, and mixtures thereof.

15. The method in claim 14, wherein said step of introducing a generally un-ionized gas comprises providing a gas selected from a group consisting of ammonia, diborane, phosphine, hydrazine, monomethylhydrazine, carbon tetrafluoride , CHF_3, HCl, boron trichloride, methylsilane, hexamethyldisilane, hexamethyldisilazane, and mixtures thereof.

16. The method in claim 15, wherein said step of passivating said surface comprises exposing said surface to an ammonia gas under parameters including:

a temperature ranging from about 150 to about 600 degrees Celsius;

an ammonia gas flow of about 5 to about 1000 sccm;

an Ar gas flow of about 200 to about 2000 sccm;

a pressure ranging from about 50 millitorr to about 1 atmosphere; and

a process time no greater than about 500 seconds.

17. A method of forming a capacitor, comprising:

forming a capacitor plate, comprising:

providing a first conductive layer in a first environment;

exposing said first conductive layer to a passivation gas; and

depositing a second conductive layer over said first conductive layer.

18. The method in claim 17, wherein said step of exposing said first conductive layer to a passivation gas further comprises exposing said first conductive layer to a passivation gas *ex situ*.

19. The method in claim 17, wherein said step of exposing said first conductive layer to a passivation gas further comprises exposing said first conductive layer to silane in a second environment.

20. The method in claim 17, wherein said step of exposing said first conductive layer comprises exposing said first conductive layer to a passivation gas *in situ*.

21. The method in claim 17, wherein said step of exposing said first conductive layer comprises exposing said first conductive layer to a passivation gas while still in said first environment.

22. The method in claim 17, wherein said step of providing a first conductive layer comprises providing a first conductive layer in an oxygen-free environment; and wherein said step of exposing said first conductive layer comprises exposing said first conductive layer to a passivation gas in said oxygen-free environment.

23. The method in claim 22, wherein said step of depositing a second conductive layer comprises depositing said second conductive layer in said oxygen-free environment.

24. The method in claim 22, wherein said step of depositing a second conductive layer comprises depositing said second conductive layer in a second oxygen free-environment.

25. A method of forming a conductive line over a substrate, comprising:

depositing a conductive plug over said substrate;

depositing a nitride over said plug in an ambient atmosphere, wherein said nitride has a surface bond;

treating said surface bond; and

depositing a metal over said nitride.

26. The method in claim 25, wherein said step of treating said surface bond comprises treating said surface bond before said step of depositing a metal.

27. The method in claim 26, wherein said step of treating said surface bond further comprises treating said surface bond in said ambient atmosphere.

28. The method in claim 27, wherein said step of treating said surface bond further comprises treating said surface bond in a reducing atmosphere.

29. The method in claim 28, wherein said step of treating said surface bond further comprises inhibiting an ability of said nitride to adsorb oxygen.

30. A damascene process, comprising:

depositing a first layer of insulation over a substrate;

etching a first hole in said first layer of insulation;

filling said first hole with a metal;

depositing a second layer of insulation over said first layer of insulation;

etching a second hole in said second layer of insulation and over said first hole;

providing an interface layer over said metal and within said second hole; and

exposing said interface layer to a nitrogen/hydrogen plasma.

31. A semiconductor process, comprising:

providing a first conductive layer;

providing a second conductive layer on said first conductive layer; and

inhibiting a formation of oxide between said first conductive layer and said second

conductive layer with a passivator material.

32. The process in claim 31, wherein said step of inhibiting a formation of oxide comprises preventing an oxygen molecule from moving from said first conductive layer to said second conductive layer.

33. The process in claim 32, wherein said step of preventing an oxygen molecule from moving from said first conductive layer comprises preventing said oxygen molecule from associating with said first conductive layer.

34. The process in claim 33, wherein said step of providing a first conductive layer further comprises providing a first conductive layer having a bond, wherein said bond has an activity property; and wherein said step of preventing said oxygen molecule from associating with said first conductive layer comprises reducing said activity property.

35. The process in 33, wherein said step of preventing said oxygen molecule from associating with said first conductive layer comprises preventing said oxygen molecule ~~from being adsorbed onto said first conductive layer~~.

36. A method of forming a semiconductor device, comprising:

depositing a first conductive layer having a surface;

incorporating an oxygen-free material into said surface;

depositing a second conductive layer on said surface; and

exposing said second conductive layer to a thermal process.

37. The method in claim 36, wherein:

said step of depositing a first conductive layer comprises depositing a capacitor plate;

said method further comprises depositing an insulator over said second conductive layer; and

said step of exposing said second conductive layer to a thermal process comprises flowing said insulator.

38. The method in claim 36, wherein:

said step of depositing a first conductive layer comprises depositing a plug; and

said step of exposing said second conductive layer to a thermal process comprises flowing said second conductive layer.

39. The method in claim 36, wherein said step of exposing said second conductive layer to a thermal process comprises exposing said second conductive layer to an alloy process.

40. A method of constructing a multi-layered device, comprising:

providing a first conductive layer in a first environment;

protecting said first conductive layer from oxygen association, wherein said protecting step is accomplished with a second environment formed of a gas selected from a group consisting of:

a plasma,

a non-ionized gas,

a nitrogen-containing gas,

a nitrogen-free gas,

an *in situ* gas,

an *ex situ* gas, and

combinations thereof; and

providing a second conductive layer on said first conductive layer.

41. A method of processing a semiconductor device, comprising:

depositing a first conductive material;

introducing said first conductive material to a nitrogen-containing plasma;

depositing a second conductive material over said first conductive material; and

exposing said first conductive material and said second conductive material to a thermal process.

42. The method in claim 41, wherein said step of exposing said first conductive material and said second conductive material to a thermal process further comprises developing an oxide between said first conductive material and said second conductive material, wherein said oxide is less than 10 angstroms thick.

43. A method of passivating a multilayer conductive structure, comprising:

layering a first conductive material;

introducing a selection of N_2/H_2, N_2, and NH_3 gas to said first conductive material;

releasing nitrogen from said gas with electromagnetic energy; and

layering a second conductive material over said first conductive material.

44. The method in claim 43, wherein said step of releasing nitrogen from said gas with electromagnetic energy comprises directing ultraviolet light toward said gas.

45. A method of treating a wafer, comprising:

depositing a first conductive layer onto said wafer;

exposing said wafer in situ to a reducing environment; and

depositing a second conductive layer.

46. The method in claim 45, wherein said step of exposing said wafer in situ to a reducing environment comprises exposing said wafer to silane gas.

47. The method in claim 46, further comprising a step of exposing said wafer in situ to an N_2/H_2 plasma prior to said step of depositing a second conductive layer.

48. The method in claim 47, wherein said step of exposing said wafer in situ to an N_2/H_2 plasma comprises exposing said wafer in situ to said N_2/H_2 plasma prior to said step of exposing said wafer to silane gas.

49. A method of processing a wafer, comprising:

depositing a first conductive layer having a grain boundary; and

associating a non-oxygen material with said grain boundary by exposing said first conductive layer to a selection consisting of:

an N_2/H_2 plasma,

an N_2 plasma,

an H_2 plasma,

an NH_3 plasma,

an NH_3 non-plasma gas,

a silane gas, and

a combination thereof.

50. The method in claim 49, wherein said step of depositing a first conductive layer further comprises depositing a tungsten nitride layer.

51. The method in claim 50, further comprising a step of depositing a second conductive layer over said first conductive layer.

52. The method in claim 50, further comprising a step of depositing a dielectric over said first conductive layer.

53. The method in claim 52, further comprising:

depositing a second conductive layer over said dielectric; and

exposing said second conductive layer to a selection consisting of:

an N_2/H_2 plasma,

an N_2 plasma,

an H_2 plasma,

an NH_3 plasma,

an NH_3 non-plasma gas,

a silane gas, and

a combination thereof.

54. A method of forming a semiconductor device, comprising:

providing a first conductive layer; and

preventing at least some oxygen from migrating in relation to said first conductive layer.

55. The method in claim 54, wherein said method further comprises providing a dielectric onto said first conductive layer; and wherein said step of preventing at least some oxygen from migrating comprises preventing at least some oxygen from migrating from said dielectric to said first conductive layer.

56. The method in claim 54, wherein said method further comprises providing a second conductive layer onto said first conductive layer; and wherein said step of preventing at least some oxygen from migrating comprises preventing at least some oxygen from migrating from said first conductive layer to said second conductive layer.

57. A semiconductor device, comprising:

a substrate;

a first conductive layer over said substrate;

a dielectric over said substrate;

a second conductive layer over said first conductive layer; and

a non-oxygen material between said first conductive layer and said second

conductive layer.

58. The semiconductor device of claim 57, wherein:

said dielectric is over said first conductive layer;

said second conductive layer is over said dielectric; and

said non-oxygen material is between said first conductive layer and said dielectric.

59. The semiconductor device of claim 57, wherein said first conductive layer is over said dielectric.

60. The semiconductor device of claim 59, further comprising a third conductive layer between said substrate and said dielectric.

61. A capacitor, comprising:

a bottom plate comprising tungsten nitride and having a surface;

nitrogen at said surface;

a dielectric comprising tantalum pentoxide over said surface; and

a top plate over said dielectric.

62. A capacitor, comprising:

a first plate;

a dielectric over said first plate; and

a second plate over said dielectric, comprising:

a first non-polysilicon conductive layer over said dielectric, and

a second conductive layer over said first non-polysilicon conductive layer.

63. The capacitor in claim 62, wherein said dielectric contains oxygen; wherein said first non-polysilicon conductive layer contains nitrogen; and wherein said second conductive layer comprises polysilicon.

64. The capacitor in claim 63, wherein:

said dielectric layer consists of a selection from tantalum pentoxide and barium strontium titanate; and

said first non-polysilicon conductive layer consists of a selection from tungsten nitride and tantalum nitride.

65. The capacitor in claim 64, wherein said second plate comprises an oxygen-free second plate.

66. The capacitor in claim 64, wherein said second plate comprises an oxide layer between said first non-polysilicon conductive layer and said second conductive layer, wherein said oxide layer is less than 10 angstroms thick.

67. The capacitor in claim 64, wherein said first non-polysilicon conductive layer and said second conductive layer are less than 10 angstroms apart and are separated by a silicon dioxide layer.

68. A pair of series-coupled capacitors, comprising:

a first conductive layer;

a dielectric over said first conductive layer;

a second conductive layer over said dielectric;

a third conductive layer less than 10 angstroms over said second conductive layer; and

an oxide of said third conductive layer between said second conductive layer and said third conductive layer.

69. The pair of series-coupled capacitors in claim 68, wherein said first conductive layer, said dielectric, and said second conductive layer define a first capacitor; and wherein said second conductive layer, said oxide, and said third conductive layer define a second capacitor.

70. A semiconductor device, comprising:

a conductive line;

a plug under said conductive line; and

an interposing layer between said conductive line and said plug and comprising a non-oxygen stuffing material.

71. The semiconductor device in claim 70, wherein said interposing layer comprises grain boundaries and nitrogen between said grain boundaries.

72. The semiconductor device in claim 71, further comprising an oxide between said interposing layer and said conductive line.

73. An in-process device, comprising:

a substrate; and

a conductive layer over said substrate and having a surface stuffed with a non-oxygen material.

74. The in-process device of claim 73, wherein said surface is a nitrogen-stuffed surface.

75. The device in claim 74, wherein said surface is contacting an oxygen molecule.